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(12) **United States Patent**  
**Tanaka et al.**

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(45) **Date of Patent:** **\*Jun. 26, 2001**

(54) **METHOD OF USING PHOSPHOROUS TO  
GETTER CRYSTALLIZATION CATALYST IN  
A P-TYPE DEVICE**

(75) **Inventors:** **Koichiro Tanaka; Hideto Ohnuma,**  
both of Kanagawa (JP)

(73) **Assignee:** **Semiconductor Energy Laboratory  
Co., Ltd., Kanagawa-ken (JP)**

(\*) **Notice:** This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/334**

(52) **U.S. Cl.** ..... **438/143; 438/154**

(58) **Field of Search** ..... 438/152, 153,  
438/151, 150, 149, 142, 143, 471, 473,  
154; 257/57, 64, 65, 66, 75

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*Primary Examiner*—Charles Bowers

*Assistant Examiner*—Evan Pert

(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

A method for producing a thin-film transistor by using a crystalline silicon film that has been formed by using nickel as a metal element for accelerating crystallization of silicon. In forming source and drain regions, phosphorus as an element for gettering nickel is introduced therein by ion implantation. Nickel gettering is effected by annealing. For example, in the case of producing a P-channel thin-film transistor, both phosphorus and boron are used. Boron determines a conductivity type, and phosphorus is used as a gettering material.

**30 Claims, 4 Drawing Sheets**

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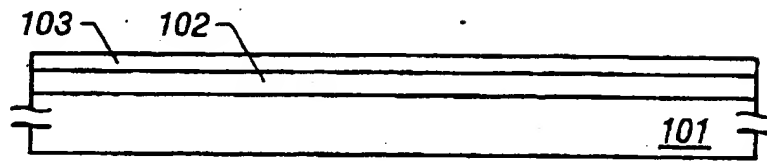


FIG. 1A

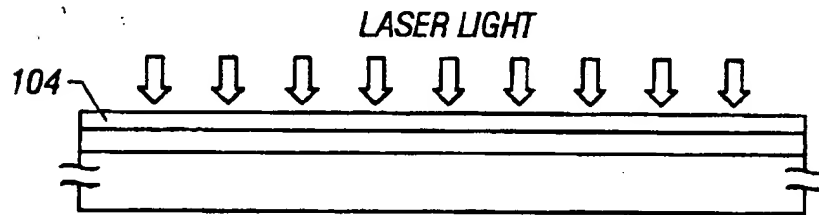


FIG. 1B

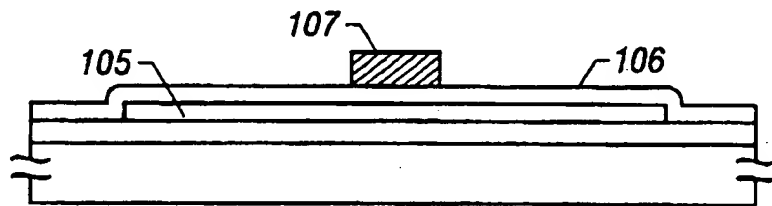


FIG. 1C

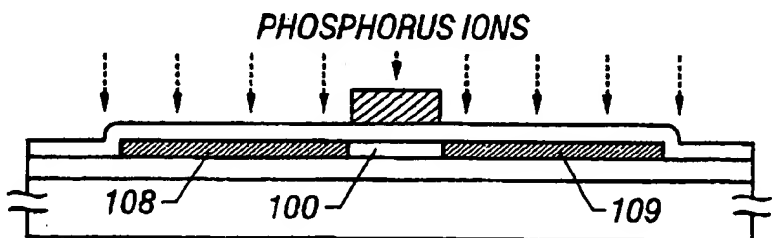


FIG. 1D

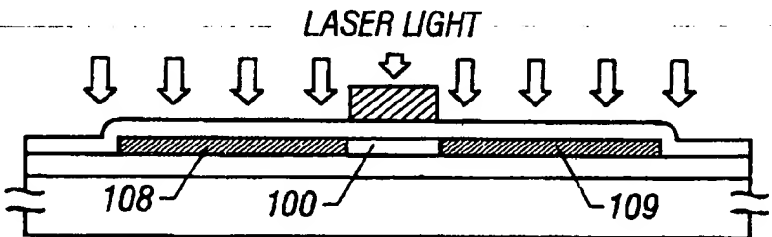


FIG. 1E

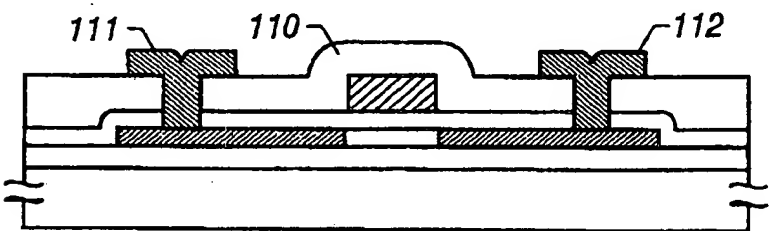


FIG. 1F

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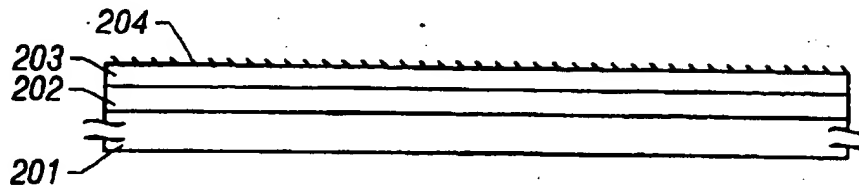


FIG. 2A

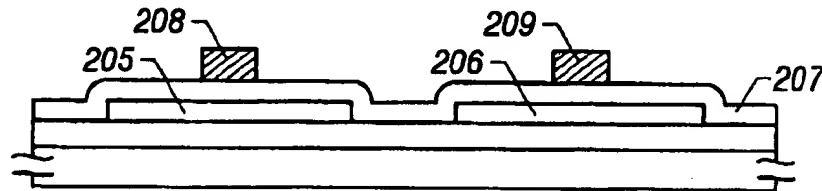


FIG. 2B

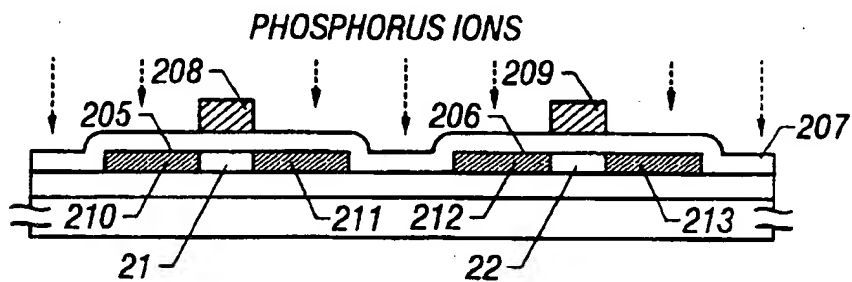


FIG. 2C

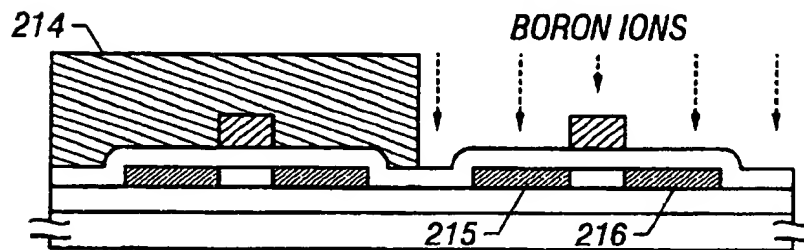


FIG. 2D

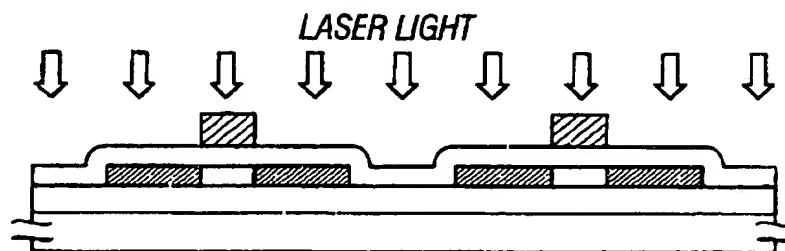


FIG. 2E

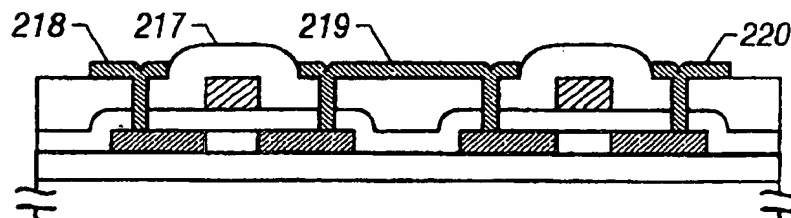


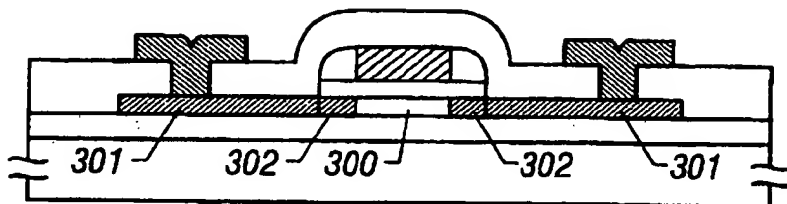
FIG. 2F

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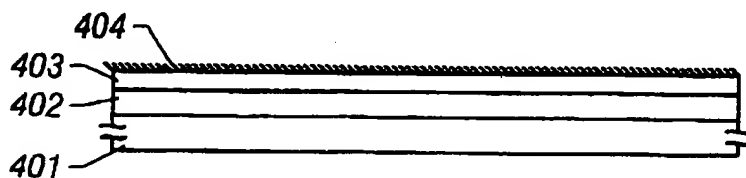
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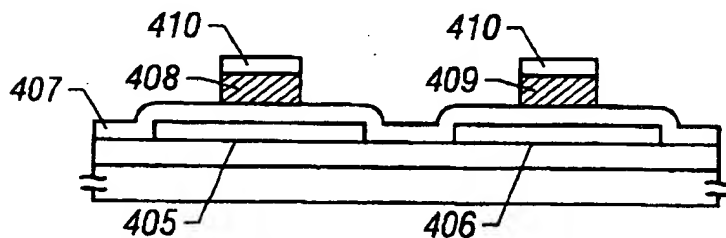
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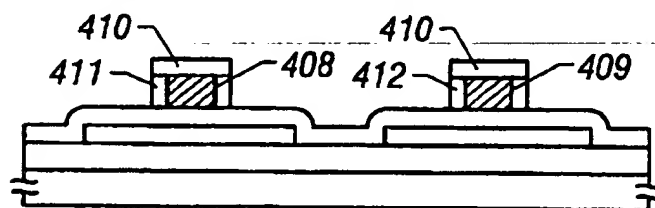
**FIG. 3**



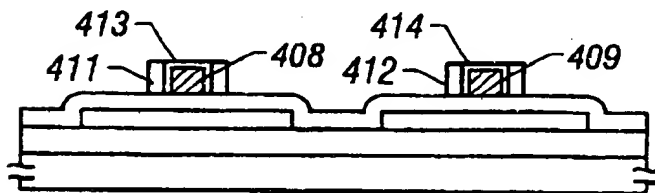
**FIG. 4A**



**FIG. 4B**



**FIG. 4C**



**FIG. 4D**

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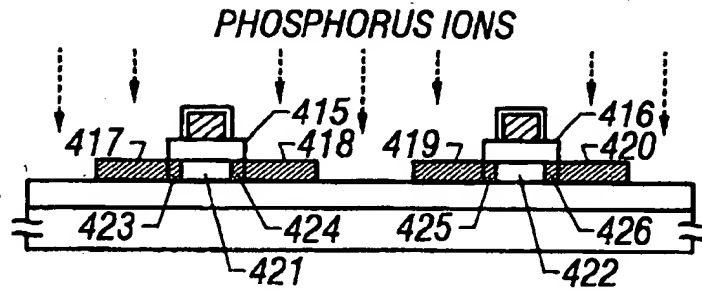


FIG. 4E

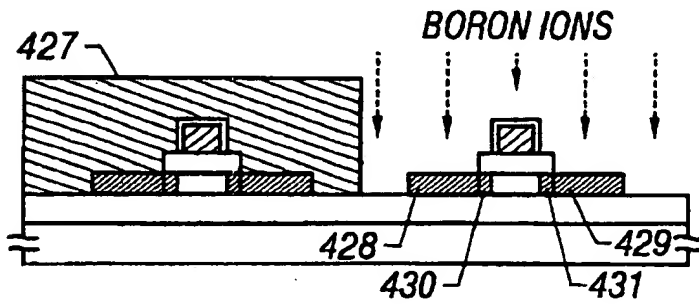


FIG. 4F

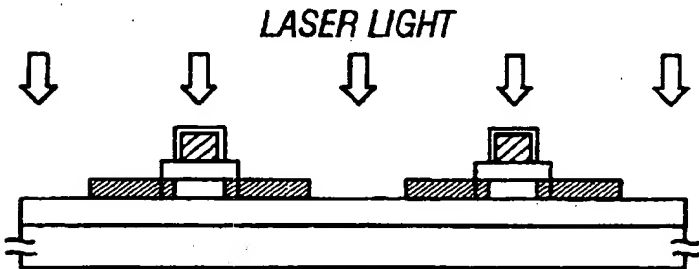


FIG. 4G

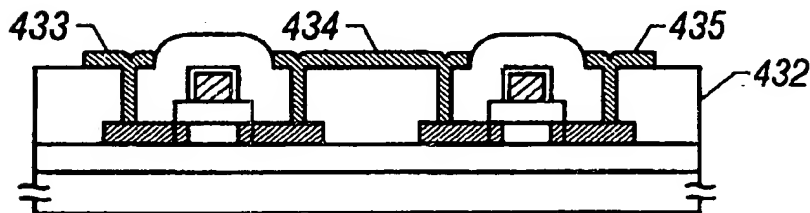


FIG. 4H

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# METHOD OF USING PHOSPHOROUS TO GETTER CRYSTALLIZATION CATALYST IN A P-TYPE DEVICE

This is a divisional of copending application Ser. No. 08/622,828, filed Mar. 27, 1996.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a doping technique in a manufacturing process of an insulated-gate semiconductor device, such as a thin-film transistor (TFT), having a non-single-crystal crystalline silicon film and other semiconductor devices which doping technique minimizes adverse effects on such a device of an impurity (e.g., Ni) contained in the crystalline silicon film. The invention is particularly advantageous when the crystalline silicon film is one that has been formed with the aid of a crystallizing catalyst element (e.g., Ni).

### 2. Description of the Related Art

In recent years, various studies have been made of insulated-gate semiconductor devices having a thin-film active layer (active region) on an insulative substrate. In particular, a thin-film, insulated-gate transistor, i.e., what is called a thin-film transistor (TFT) has been studied enthusiastically. Thin-film transistors are classified into an amorphous silicon TFT, a crystalline silicon TFT, etc. depending on the material and the crystal state of a semiconductor used. Since "crystalline silicon" mentioned above in non-single-crystal silicon, the above TFTs are generically called non-single-crystal TFTs.

In general, amorphous semiconductors have small electric field mobilities, and therefore cannot be used for a TFT that is required to operate at high speed. Further, P-type amorphous silicon has a very small electric field mobility, which means that amorphous silicon cannot provide a P-channel TFT (PMOS TFT). Therefore, amorphous silicon does not allow formation of a complementary MOS (CMOS) circuit by combining P-channel TFTs and N-channel TFTs (NMOS TFTs).

On the other hand, crystalline semiconductors have larger electric field mobilities than amorphous semiconductors, and hence enable high-speed operation. Since crystalline silicon can provide a PMOS TFT as well as an NMOS TFT, it allows formation of a CMOS circuit.

A non-single-crystal crystalline silicon film can be obtained by thermally annealing, for a long time at a proper temperature (usually more than 600° C.), an amorphous silicon film that has been produced by vapor-phase growth, or by application of strong light such as laser light (optical annealing).

In the thermal annealing method, as described in Japanese Unexamined Patent Publication No. Hei. 6-244104, a crystalline silicon film can be obtained by a thermal annealing process that is shorter and lower in temperature than usual cases by using an effect that an element such as nickel, iron, cobalt, platinum, palladium, or the like (hereinafter called a crystallizing catalyst element or simply a catalyst element) accelerates crystallization of amorphous silicon.

Similar techniques are disclosed in Japanese Unexamined Patent Publication Nos. Hei. 6-318701, 6-333951, etc. It has also been revealed that in a silicon film having such a crystallizing catalyst element, thermal annealing that is lower in temperature than conventional cases enables activation of an impurity element which is performed after

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impurity regions such as a source and a drain are formed by implanting N-type or P-type impurity ions by ion doping or the like. (Japanese Unexamined Patent Publication Nos. Hei. 6-267980 and Hei. 6-267989)

For the above purpose, it is desired that the concentration of a crystallizing catalyst element be  $1 \times 10^{15}$  to  $1 \times 10^{19}$  atoms/cm<sup>3</sup>. Crystallization is not accelerated if the concentration is lower than this range, while the characteristics of a silicon semiconductor are impaired if the concentration is higher than this range. It is noted that the concentration of a catalyst element is defined as a maximum of values obtained by an analysis according to the secondary ion mass spectrometry (SIMS). In many cases, a catalyst element is distributed in a film.

Although semiconductor devices produced by using a crystalline silicon film containing a catalyst element for accelerating crystallization have a large electric field mobility, many of those exhibit a large off-current. In particular, where a large number of semiconductor devices are formed on the same substrate, large off-currents, which in itself are undesirable, have a large variation among the semiconductor devices.

Large off-currents and their large variation are believed due to the existence of the catalyst element for accelerating crystallization; that is, mainly due to the fact that the catalyst element exists in junctions.

In particular, the above undesired characteristics are fatal to TFTs that constitute a pixel section of a liquid crystal display.

## SUMMARY OF THE INVENTION

Among semiconductor devices produced by using a crystalline silicon film into which nickel was introduced as a catalyst element for accelerating crystallization, those whose impurity regions (sources and drains, etc.) were formed by implanting phosphorus showed relatively low off-currents (about 10 pA or less) with almost no variation. Based on this fact, the inventors have studied properties of phosphorus in detail, and have found a report stating that phosphorus has a feature of gettering impurities.

According to this report, phosphorus shows a particularly high degree of gettering function with respect to nickel. Further, element, such as copper and iron, which are considered to adversely affect semiconductor devices, can be gettering by phosphorus. This leads to an assumption that in the above semiconductor devices, phosphorus neutralizes the properties of nickel in a certain manner, to thereby suppress the adverse effects of nickel on the off-current characteristic.

The invention utilizes the gettering function of phosphorus with respect to nickel. "The gettering function" is defined as an operation that phosphorus captures nickel, thereby reducing the effect of nickel.

For example, a process for manufacturing an n-channel type thin film transistor using the nickel function will be explained as follows.

First, source and drain regions are formed by doping phosphorus ions using a gate electrode as a mask.

A channel region and n-type source and drain regions are formed in an active region of the thin film transistor by the phosphorus ion doping.

After that, thermal annealing or laser annealing is performed. In this process, nickel elements are removed from the channel region that no phosphorus is doped by the function of phosphorus doped in the source and drain

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regions. That is, the nickel elements are captured by phosphorus and thereby the nickel elements are transferred from the channel region into the source and drain regions.

In the result of the thermal annealing or laser annealing process described above, the nickel elements gather into the source and drain regions. On the other hand, nickel elements are reduced in the region that no phosphorus is doped. The nickel element doped highly in the channel region affects operation of the thin film transistor adversely.

In operation of the thin film transistor, it is required that resistance of the channel region is slightly changed by a voltage applied for the gate electrode. That is, slight change of electric property is needed for the channel region. However, the nickel disturbs the slight change.

Consequently, the Off-current is increased and the characteristics of the thin film transistor fluctuates.

On the other hand, even if nickel is highly doped in the source and drain regions, the off-current is not almost increased and the characteristic does not almost affect.

Accordingly, it is excessively effective for enhancing the characteristic of the thin film transistor to change distribution of nickel in the active region, that is, to increase concentration of nickel in source and drain regions and reduce concentration thereof in the channel region, relatively.

Where a p-channel type film transistor is manufactured, phosphorus ions are doped into the source and drain regions and p-type impurities are doped therein to invert the conductivity type. Thereby, the nickel is transferred into the source and drain regions.

In the invention described above, the catalyst element for accelerating crystallization may be a metal element such as nickel, platinum, cobalt, iron, palladium, or the like. Among those elements, nickel is particularly superior in the effect of accelerating crystallization of silicon.

It is preferred that the concentration of the catalyst element be set in a range of  $1 \times 10^{15}$  to  $1 \times 10^{19}$  atoms/cm<sup>3</sup>. If the concentration is lower than  $1 \times 10^{15}$  atoms/cm<sup>3</sup>, the effect of accelerating crystallization is not attained. On the other hand, if the concentration is higher than  $1 \times 10^{19}$  atoms/cm<sup>3</sup>, silicon partly assumes metallic properties to lose its semiconductor characteristics. It is noted that in this specification the concentration of a catalyst element in a silicon film is defined as a maximum of values obtained by an analysis and a measurement according to the secondary ion mass spectrometry (SIMS).

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 1F show a manufacturing process of a thin-film transistor according to first and second embodiments of the present invention;

FIGS. 2A to 2F show a manufacturing process of a thin-film transistor according to a third embodiment of the invention;

FIG. 3 shows a thin-film transistor according to a fourth embodiment of the invention; and

FIGS. 4A to 4H show a manufacturing process of a thin-film transistor according to a seventh embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

## Embodiment 1

This embodiment is directed to a method of producing an N-type semiconductor device having superior characteristics

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by forming an uncompleted transistor on a crystalline silicon film into which nickel as a catalyst element for accelerating crystallization has been introduced, then implanting ions including phosphorus ions into its source and drain regions by known ion doping (also called plasma doping) or ion implantation, and finally improving the crystallinity of the silicon film and activating impurities by thermal annealing or optical annealing (or both). In the following, "semiconductor devices having superior characteristics" means semiconductor devices in which off-currents are about 10 pA or less and variations of characteristics among devices are small. FIGS. 1A to 1F show a manufacturing process of this embodiment.

First, a 2,000-Å-thick undercoat silicon oxide film 102 and a 500-Å-thick amorphous silicon film 103 are sequentially formed on a glass substrate (Corning 7059 in this embodiment) 101 by plasma CVD. A nickel acetate layer (not shown) is formed on the above structure by applying a nickel acetate aqueous solution of 10 ppm and performing spin coating. It is preferred that a surface active agent be added to the nickel acetate aqueous solution. (FIG. 1A)

Thereafter, thermal annealing is performed at 550° C. for 4 hours to crystallize the amorphous silicon film 103, i.e., obtain a crystalline silicon film 104. In this process, nickel serves as crystal nuclei, thereby accelerating crystallization of the amorphous silicon film 103.

It is due to this action of nickel that the above thermal annealing can be performed under the low-temperature (lower than the strain temperature of Corning 7059), short-time conditions of 550° C. and 4 hours. Details of the above steps are described in Japanese Unexamined Patent Publication No. Hei. 6-244104.

It is preferred that the concentration of the catalyst element be set in a range of  $1 \times 10^{15}$  to  $1 \times 10^{19}$  atoms/cm<sup>3</sup>. In this embodiment, the concentration of the catalyst element in the silicon film is  $1 \times 10^{17}$  to  $5 \times 10^{18}$  atoms/cm<sup>3</sup> in terms of a minimum value in the film, which concentration is defined as a maximum of values obtained by an analysis and a measurement according to the secondary ion mass spectrometry (SIMS).

To improve the crystallinity of the above-obtained crystalline silicon film 104, it is illuminated with light emitted from an excimer laser that is a high-power pulsed laser. In this embodiment, a KrF excimer laser (wavelength: 248 nm; pulse width: 30 nsec) is used. The energy density of laser light is selected from a range of 100 to 500 mJ/cm<sup>2</sup> so as to provide the crystalline silicon film 104 with best crystallinity. In this embodiment, the laser light energy density is set at 370 mJ/cm<sup>2</sup>. Where the area of an illumination object is larger than the beam size of the excimer laser light, the illumination is performed while the laser beam is moved relative to the illumination object. The illumination is so performed that each point on the illumination object receives 2 to 20 shots of laser light. The substrate temperature is kept at 200° C. during the laser light illumination. (FIG. 1B)

Then, the crystalline silicon film 104 is etched into an island-like silicon region 105. A 1,200-Å-thick silicon oxide film 106 as a gate insulating film is deposited thereon by plasma CVD using TEOS as a material gas, with the substrate temperature kept at 250 to 380° C., for instance, 300° C. (FIG. 1C)

Subsequently, an aluminum film (containing silicon at 0.1 to 2%) is deposited by sputtering at a thickness of 3,000 to 8,000 Å, for instance, 6,000 Å, and then etched to form a gate electrode 107. (FIG. 1C)

Thereafter, phosphorus ions are implanted into the island-like silicon region 105 with the gate electrode 107 used as

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a mask. Phosphine ( $\text{PH}_3$ ) that is diluted with hydrogen to 1 to 10% is used as a doping gas. The acceleration voltage is set at 60 to 90 kV, for instance, 80 kV, and the dose is set at  $1 \times 10^{13}$  to  $8 \times 10^{15}$  atoms/cm<sup>2</sup>, for instance,  $2 \times 10^{14}$  atoms/cm<sup>2</sup>. Under these conditions, phosphorus ions are introduced into the island-like region 105 at a concentration of  $3 \times 10^{19}$  atoms/cm<sup>3</sup>. Thus, N-type impurity regions 108 (source) and 109 (drain) and a channel region 100 are formed. (FIG. 1D)

According to the experiences of the inventors, the preferable range of concentration of an impurity for imparting N-type or P-type conductivity in a silicon region is  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>. The substrate is kept at the room temperature during the ion doping.

Then, to activate phosphorus (dopant) and to cause phosphorus to getter nickel, optical annealing is performed by using a KrF excimer laser. The energy density of laser light is set at 100 to 350 mJ/cm<sup>2</sup>, for instance, 250 mJ/cm<sup>2</sup>. Where the area of an illumination object is larger than the beam size of excimer laser light, the illumination is performed while the laser beam is moved relative to the illumination object. The illumination is so performed that each point on the illumination object receives 2 to 20 shots of laser light. The substrate temperature is kept at 200° C. during the laser light illumination. Then, thermal annealing is performed at 350° C. for 2 hours in a nitrogen atmosphere. Although both optical annealing and thermal annealing are performed in this embodiment, only one of those may be performed.

In the annealing process, nickel in the channel region 100 is transferred into the source region 108 and drain region 109. Thereby, concentration of nickel in the channel region 100 can be reduced. (FIG. 1E)

Subsequently, a 6,000-Å-thick silicon oxide film 110 as an interlayer insulating film is deposited by plasma CVD, and contact holes are formed therein. After a metal material, for instance, a multi-layer film of titanium and aluminum films is deposited and patterned to form electrode/wiring lines 111 and 112 of the source and drain of a TFT. Finally, thermal annealing is performed at 200 to 350° C. in a hydrogen atmosphere of 1 atm. (FIG. 1F)

## Embodiment 2

This embodiment is directed to a method of producing a P-type semiconductor device having superior characteristics in a process of manufacturing a transistor by using a crystalline silicon film into which nickel as a catalyst element for accelerating crystallization has been introduced. More specifically, ions including phosphorus ions are implanted into source and drain regions of the crystalline silicon film by known ion doping (also called plasma doping), then a P-type impurity ions (in this embodiment, ions including boron ions) are further implanted into the silicon film, and finally thermal annealing or optical annealing (or both) is performed to improve the crystallinity of the silicon film and activate impurities.

This embodiment may be implemented by adding a step of implanting P-type impurity ions (in this embodiment, ions including boron ions) into the source and drain regions. This step may be performed before or after the phosphorus ion doping shown in FIG. 1D. Only the additional step of doping with P-type impurity ions will be described below.

In this embodiment, boron ions as P-type impurity ions are implanted into the silicon region 105 with the gate electrode 107 used as a mask. Diborane ( $\text{B}_2\text{H}_6$ ) that has been diluted with hydrogen to 5% is used as a doping gas. The acceleration voltage is set at 60 to 90 kV, for instance, 80 kV, and the dose is set at  $1 \times 10^{13}$  to  $8 \times 10^{15}$  atoms/cm<sup>2</sup>, for instance,  $4 \times 10^{14}$  atoms/cm<sup>2</sup>.

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In this step, the dose is so adjusted that the maximum concentration value of boron in the source and drain regions minus that of phosphorus in the same regions becomes  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>. The substrate is kept at the room temperature during the ion doping. Thus, P-type impurity regions 108 (source) and 109 (drain) and channel region 100 are formed.

In this embodiment, in forming the P-type TFT, not only the impurity for imparting P-type conductivity such as boron but also nickel and phosphorus are added to the active layer made of a crystalline silicon film. Therefore, a silicon film having good crystallinity can be obtained at a low temperature in a short time due to the catalyst effect of nickel, and nickel that has become unnecessary can be getterd by phosphorus. As a result, this embodiment can produce TFTs having superior electrical characteristics whose variations among devices are small.

That is, concentration of nickel in the channel region 100 can be reduced. Thereby, the thin film transistor having high characteristics and low fluctuation thereof can be obtained.

## Embodiment 3

This embodiment is directed to a method of separately producing N-type and P-type semiconductor devices having superior characteristics on the same substrate by forming a plurality of uncompleted transistors on a crystalline silicon film into which nickel as a catalyst element for accelerating crystallization, then implanting ions including phosphorus ions into their source and drain regions by known ion doping (also called plasma doping), and finally selectively implanting P-type impurity ions (in this embodiment, ions including boron ions).

FIGS. 2A to 2F shows a manufacturing process of CMOS TFTs according to this embodiment. First, as shown in FIG. 2A, an undercoat silicon oxide film 202 is deposited on a glass substrate (Corning 1737) 201 at a thickness of 1,000 to 5,000 Å, for instance, 2,000 Å, by plasma CVD using monosilane and nitrogen monoxide as materials. A 1,000-Å-thick amorphous silicon film 203 is deposited thereon by plasma CVD using monosilane as a material.

Thereafter, a very thin silicon oxide film (not shown) is formed on the surface of the amorphous silicon film 203 by using an aqueous solution of hydrogen peroxide. An acetate salt solution containing nickel at 1 to 30 ppm, for instance, 10 ppm, is applied by spin coating and then dried to form a catalyst layer 204 containing nickel. (FIG. 2A)

Subsequently, thermal annealing is performed at 550° C. for 4 hours in a nitrogen atmosphere to crystallize the amorphous silicon film 203. In this process, nickel moves from the amorphous silicon film 203 to the undercoat silicon oxide film 202, and crystallization proceeds downward.

After the crystallization step by thermal annealing, XeCl laser light (wavelength: 308 nm) is applied to the crystallized silicon film to enhance its crystallinity.

Then, as shown in FIG. 2B, the crystallized silicon film is etched into island-like silicon regions 205 and 206. A 1,000-Å-thick silicon oxide film 207 as a gate insulating film is deposited thereon by plasma CVD using monosilane and nitrogen monoxide as materials.

Subsequently, an aluminum film (containing scandium at 0.1 to 2%) is deposited by sputtering at a thickness of 3,000 to 8,000 Å, for instance, 4,000 Å, and then etched to form gate electrodes 208 and 209.

Then, as shown in FIG. 2C, the island-like silicon regions 205 and 206 are doped with phosphorus ions by ion doping



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in a self-aligned manner with the gate electrodes 208 and 209 used as a mask. Phosphine ( $\text{PH}_3$ ) that is diluted with hydrogen to 1 to 10% is used as a doping gas. The acceleration voltage may be set at 60 to 90 kV, and the dose may be set at  $1 \times 10^{13}$  to  $8 \times 10^{13}$  atoms/cm<sup>3</sup>. In this embodiment, the acceleration voltage is set at 80 kV, and the dose is set at  $2 \times 10^{14}$  atoms/cm<sup>3</sup>. Under these conditions, phosphorus ions are introduced into the island-like silicon regions 205 and 206 at a concentration of  $3 \times 10^{19}$  atoms/cm<sup>3</sup>, so that N-type impurity regions 210 to 213 are formed.

Thereafter, as shown in FIG. 2D, a region to become an N-type TFT is covered with a resist mask 214 by a known photoresist method. In this state, P-type impurity ions (in this embodiment, boron ions) are introduced into the island-like silicon region 206 by ion doping with the gate electrode 209 used as a mask. Diborane ( $\text{B}_2\text{H}_6$ ) that is diluted with hydrogen to 5% is used as a doping gas. The acceleration voltage may be set at 60 to 90 kV, and the dose may be set at  $1 \times 10^{13}$  to  $8 \times 10^{15}$  atoms/cm<sup>3</sup>. In this embodiment, the acceleration voltage is set at 80 kV and the dose is set at  $4 \times 10^{14}$  atoms/cm<sup>3</sup>. As a result, the conductivity type of the N-type impurity regions 212 and 213 of the island-like silicon region 206 is inverted to form P-type impurity regions 215 (source) and 216 (drain). On the other hand, the N-type conductivity of the impurity regions 210 and 211 that are covered with the resist mask 214 is maintained.

In the above step, the dose is so adjusted that the maximum concentration of boron in the source and drain regions 215 and 216 minus that of phosphorus in those regions becomes  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>. The substrate is kept at the room temperature during the ion doping.

Although in this embodiment boron ions are introduced after the phosphorus ion implantation, they may be introduced before the phosphorus ion implantation. In the latter case, as shown in FIG. 2D, boron ions are introduced in a state that the N-type TFT region is covered with a mask 214. Phosphorus ions may be introduced after the resist mask 214 is removed.

Then, after the resist mask 214 is removed, laser annealing is performed as shown in FIG. 2E to activate the added impurities and to restore the crystallinity of the island-like silicon regions 205 and 206 that have been damaged in the doping step. In this embodiment, since phosphorus is added to the N-type impurity regions 210 and 211 and the P-type impurity regions 215 and 216 at a concentration of  $3 \times 10^{19}$  atoms/cm<sup>3</sup>, nickel is getter by phosphorus upon laser light illumination. KrF excimer laser light (wavelength: 248 nm) is used. To getter nickel effectively, it is preferred that the laser light illumination conditions be such that the energy density is 200 to 400 mJ/cm<sup>2</sup>, for instance, 250 mJ/cm<sup>2</sup>, each point receives 2 to 20 shots of laser light, and the substrate temperature during the laser light illumination is set at 200° C.

In this process, nickel in the channel regions 21 and 22 is transferred into the source and drain regions 210, 211, 212 and 213 that phosphorus is doped. Thereby, concentration of nickel in the channel region 21 and 22 can be reduced.

After the laser annealing, thermal annealing is performed at 350° C. for 2 hours in a nitrogen atmosphere. Although both laser annealing and thermal annealing are performed in this embodiment, only one of those may be performed.

Subsequently, as shown in FIG. 2F, a 6,000-Å-thick silicon oxide film 216 as an interlayer insulating film is formed by plasma CVD. After contact holes are formed in the interlayer insulating film 217, electrodes/wiring lines 218 to 220 of the N-type and P-type TFTs are formed by

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using a metal material, for instance, a multi-layer film of titanium film and an aluminum film. Finally, a thermal treatment is performed at 350° C. for 2 hours in a hydrogen atmosphere. (FIG. 2F)

With the above steps, CMOS TFTs are completed in which the N-type TFT and the P-type TFT are combined complementarily.

## Embodiment 4

This embodiment is directed to a method of producing an N-type semiconductor device having superior characteristics in manufacturing a thin-film transistor having a LDD structure by using a crystalline silicon film into which nickel as a catalyst element for accelerating crystallization has been introduced. More specifically, ions including phosphorus ions are implanted into source and drain regions and LDD regions by known ion doping (also called plasma doping), and then thermal annealing or optical annealing (or both) is performed to improve the crystallinity of the silicon film and activate impurities.

The same steps as in the first embodiment are employed until formation of a crystalline silicon film. Thereafter, a thin-film transistor having a known LDD structure is formed by a known method. The source and drain regions and the LDD regions are activated in the same manner as in the first embodiment. FIG. 3 shows a TFT of a LDD structure having side walls.

As shown in FIG. 3, lightly doped impurity regions 302 having a lower impurity concentration than source and drain regions 301 are formed between the source and drain regions 301 and the channel regions. One of the lightly doped impurity regions 302 which is located on the drain side is particularly called a LDD region.

In this embodiment, phosphorus is implanted in the source and drain regions 301 at  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, and it is implanted in the lightly doped impurity regions 302 at  $4 \times 10^{16}$  to  $7 \times 10^{17}$  atoms/cm<sup>3</sup>. With the doping of such concentrations, phosphorus can effectively getter nickel that has become unnecessary. Therefore, TFTs can be obtained in which the characteristics have only small variations among devices and off-currents are small.

## Embodiment 5

This embodiment is directed to a method of producing a P-type semiconductor device having superior characteristics in manufacturing a thin-film transistor having a LDD structure by using a crystalline silicon film into which nickel as a catalyst element for accelerating crystallization has been introduced. More specifically, ions including phosphorus ions are implanted into LDD regions by known ion doping (also called plasma doping), then P-type impurity ions are implanted into source and drain regions and the LDD regions, and finally thermal annealing or optical annealing (or both) is performed to improve the crystallinity of the silicon film and activate impurities.

Manufacturing steps of this embodiment are almost the same as those in the fourth embodiment. This embodiment is different from the fourth embodiment in that the LDD regions 302 are doped with boron, as well as phosphorus, at a concentration of  $3 \times 10^{17}$  to  $3 \times 10^{18}$  atoms/cm<sup>3</sup> that is higher than that of phosphorus. The doping of boron inverts the conductivity type of the LDD regions 302 from an N-type to a P-type. The source and drain regions 301 are doped with boron, instead of phosphorus, at  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, and therefore assume P-type conductivity.

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The concentration of phosphorus in the LDD regions 302 is lower than that of boron in the source and drain regions 301 by 2 to 4 orders, the conductivity type of the LDD regions 302 can be inverted from an N-type to a P-type by introducing boron at a lower dose than that of the source and drain regions 301 is inverted. In inverting the conductivity type of the LDD regions 302 from an N-type to a P-type, the dose is so adjusted that the maximum concentration of boron implanted in the LDD regions 302 minus that of phosphorus implanted in those regions becomes  $3 \times 10^{17}$  to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.

In this embodiment, in producing the P-type TFT, not only the impurity that imparts P-type conductivity such as boron but also nickel and phosphorus are introduced into the active layer made of a crystalline silicon film. Therefore, a silicon film having good crystallinity can be obtained at a low temperature in a short time due to the catalyst effect of nickel.

Nickel in the channel 300 is transferred into LDD regions 302 and source and drain regions 301 by the gettering function of phosphorus. Thereby, concentration of nickel in the channel region 300 can be reduced.

As a result, this embodiment can produce TFTs having superior electrical characteristics whose variations among devices are small.

## Embodiment 6

This embodiment is directed to a method of producing a P-type semiconductor device having superior characteristics in manufacturing a thin-film transistor having a LDD structure by using a crystalline silicon film into which nickel as a catalyst element for accelerating crystallization has been introduced. More specifically, ions including phosphorus ions are implanted into source and drain regions and LDD regions by known ion doping (also called plasma doping), then P-type impurity ions are implanted into the source and drain regions and the LDD regions, and finally thermal annealing or optical annealing (or both) is performed to improve the crystallinity of the silicon film and activate impurities.

Manufacturing steps of this embodiment are almost the same as those in the fifth embodiment. This embodiment is different from the fifth embodiment in that the LDD regions 302 are doped with boron at a concentration of  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup> that is higher than that of phosphorus. The LDD regions 302 are also doped with boron at a concentration of  $3 \times 10^{17}$  to  $4 \times 10^{18}$  atoms/cm<sup>3</sup> that is higher than that of phosphorus. The doping of boron inverts the conductivity type of the source and drain regions 301 and the LDD regions 302 from an N-type to a P-type.

To this end, the doping conditions of boron are so determined that the maximum concentration of boron implanted in the source and drain regions 301 minus that of phosphorus implanted in those regions becomes  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, and that the maximum concentration of boron implanted in the LDD regions 302 minus that of phosphorus implanted in those regions becomes  $3 \times 10^{17}$  to  $3 \times 10^{18}$  atoms/cm<sup>3</sup>.

In this embodiment, in producing the P-type TFT, not only the impurity that imparts P-type conductivity such as boron but also nickel and phosphorus are introduced into the active layer made of a crystalline silicon film. Therefore, a silicon film having good crystallinity can be obtained at a low temperature in a short time due to the catalyst effect of nickel, and nickel can be gettered by phosphorus. As a result, this embodiment can produce TFTs having superior electrical characteristics whose variations among devices are small.

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## Embodiment 7

This embodiment is directed to a case of forming CMOS thin-film transistors in which an N-type thin-film transistor and a P-type thin-film transistor are combined complementarily. FIGS. 4A to 4H show a manufacturing process according to this embodiment. First, a silicon oxide film 402 as an undercoat film is deposited on a glass substrate (Corning 7059 or 1737) 401 at a thickness of, for instance, 2,000 Å, and a 500-Å-thick intrinsic (I-type) amorphous silicon film 403 is deposited thereon by plasma CVD.

Then, a very thin oxide film (not shown) is formed by oxidizing the surface of the amorphous silicon film 403 by UV oxidation. This oxide film improves the surface characteristics of the amorphous silicon film 403. Thereafter, an acetate salt solution containing nickel at 1 to 30 ppm, for instance, 10 ppm, is applied by spin coating and then dried to form a nickel acetate layer 404. It is noted that the nickel acetate layer 404 forms a complete layer. (FIG. 4A)

Subsequently, thermal annealing is performed at 550° C. for 4 hours in a nitrogen atmosphere, to crystallize the amorphous silicon film 403. In this heat treatment, the nickel acetate layer 404 is decomposed, and as nickel passes through the oxide film (not shown) and diffuses from the surface of the amorphous silicon film 403 to the undercoat silicon oxide film 402, crystallization of the amorphous silicon film 403 proceeds. After completion of the crystallization step, laser light may be applied to the substrate to improve the crystallinity of the crystallized silicon film.

If a metal element such as nickel exists in a crystallized silicon film at a higher concentration than  $1 \times 10^{19}$  atoms/cm<sup>3</sup>, silicon partly assumes metallic properties to lose its semiconductor characteristics. On the other hand, if the concentration of the metal element is lower than  $1 \times 10^{15}$  atoms/cm<sup>3</sup>, the effect of accelerating crystallization is not attained. Therefore, the concentration of nickel in the crystallized silicon film needs to be in a range of  $1 \times 10^{15}$  to  $1 \times 10^{19}$  atoms/cm<sup>3</sup>. The nickel concentration of the acetate salt solution, the coating conditions of the acetate salt solution, and other conditions should be predetermined so as to attain the above nickel concentration in the crystallized silicon film.

As shown in FIG. 4B, the crystallized silicon film is etched into island-like silicon regions 405 and 406. The island-like silicon regions 405 and 406 will constitute active layers of N-type and P-type TFTs, respectively.

Thereafter, a 1,500-Å-thick silicon oxide film 407 is deposited by plasma CVD, and a 4,000-Å-thick aluminum film, which is to constitute gate electrodes 408 and 409, is deposited thereon by sputtering. Scandium is added in advance to the aluminum film at 0.2 wt % to suppress occurrence of hillocks and whiskers.

Then, the aluminum film is anodized in an electrolyte to form a dense anodic oxide film (not shown) of about 100 Å in thickness. After a photoresist mask 410 is formed on the dense anodic oxide film, the aluminum film is patterned, to form gate electrodes 408 and 409. (FIG. 4B)

As shown in FIG. 4C, the gate electrodes 408 and 409 are again anodized with the photoresist mask 410 left as it is. As an electrolyte, an acid solution containing citric acid, oxalic acid, chromic acid, or sulphuric acid at 3 to 20%, for instances, a 3%-aqueous solution of oxalic acid, is used. Since the photoresist mask 410 and the dense anodic oxide film (not shown) exist on the surface of the gate electrodes 408 and 409, porous anodic oxide films 411 and 412 are formed on only the side faces of the gate electrodes 408 and

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409. The length of the lightly doped impurity regions (LDD regions) is determined by the length of growth of the porous anodic oxide films 411 and 412, which can be controlled by the anodic oxidation processing time. In this embodiment, the porous anodic oxide films 411 and 412 are grown to have a length of 7,000 Å. (FIG. 4C)

After elimination of the photoresist mask 410, the gate electrodes 408 and 409 are again subjected to anodic oxidation, to form dense, strong anodic oxide films 413 and 414. In this embodiment, an electrolyte is prepared by neutralizing a ethylene glycol solution containing tartaric acid at 3% with an aqueous solution of ammonia to pH 6.9. (FIG. 4D)

Subsequently, a silicon oxide film 407 is etched with the porous anodic oxide films 411 and 412 and the dense anodic oxide films 413 and 414 as a mask, to form gate insulating films 415 and 416. Either wet etching or dry etching can be used as long as it can etch the silicon oxide film 407 without etching the anodic oxide films 411 to 414. In this embodiment, the silicon oxide film 407 is etched by dry etching that uses a  $\text{ClF}_3$  gas.

As shown in FIG. 4E, the dense anodic oxide films (not shown) and the porous anodic oxide films 411 and 412 are sequentially removed. The dense anodic oxide films (not shown) are removed with buffer hydrofluoric acid, and the porous anodic oxide films 411 and 412 are removed with a mixed acid of phosphoric acid, acetic acid and nitric acid. Since the porous anodic oxide films 411 and 412 can be removed easily, the dense, strong anodic oxide films 413 and 414 are never etched.

Then, impurities are implanted into the island-like silicon regions 405 and 406 by ion doping with the gate electrodes 408 and 409 used as a mask. In this embodiment, phosphine ( $\text{PH}_3$ ) that is diluted with hydrogen to 1 to 10% is used as a doping gas to implant phosphorus first. The substrate is kept at the room temperature during the doping. The doping conditions such as the acceleration voltage, the dose, and the number of times of doping are properly set so as to allow the gate insulating films 415 and 416 to serve as a semi-transmissive mask.

The exposed portions of the island-like silicon regions 405 and 406 are doped with phosphorus ions at a high concentration, to form N-type heavily doped impurity regions 417 to 420, which become source and drain regions of TFTs. Since the portions right under the gate electrodes 408 and 409 are not doped with phosphorus ions, they become channel forming regions 421 and 422. As for the portions that are covered with only the gate insulating films 415 and 416, phosphorus ions are interrupted by the gate insulating films 415 and 416 and implanted into these portions by only a small amount. Therefore, these portions constitute N-type lightly doped impurity regions 423 to 426. (FIG. 4E)

In the above doping step, the doping conditions are so set that the concentration of phosphorus ions in the N-type heavily doped impurity regions 417 to 420 becomes  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, and that the concentration of phosphorus ions in the lightly doped impurity regions 423 to 426 becomes  $4 \times 10^{16}$  to  $7 \times 10^{17}$  atoms/cm<sup>3</sup>.

Subsequently, as shown in FIG. 4F, a resist film is formed, and its portion covering the region to become a P-type TFT is removed by patterning to leave a resist mask 427. Boron as an impurity to impart P-type conductivity is then implanted by ion doping. Diborane ( $\text{B}_2\text{H}_6$ ) that is diluted with hydrogen to 5% is used as a doping gas. The substrate is kept at the room temperature during the ion doping. As a

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result, in the island-like silicon region 406, the N-type conductivity of the heavily doped impurity regions 419 and 420 and the lightly doped impurity regions 425 and 426 is inverted to P-type conductivity; that is, P-type heavily doped impurity regions 428 (source) and 429 (drain) and P-type lightly doped impurity regions 430 and 431 are formed. On the other hand, the N-type conductivity of the heavily doped impurity regions 417 (source) and 418 (drain) and the lightly doped impurity regions 423 and 424 is maintained.

The doping conditions are so determined that the concentration of boron in the P-type heavily doped impurity regions 428 and 429 (source and drain regions) becomes higher than that of phosphorus in those regions by  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, and that the concentration of boron in the P-type lightly doped impurity regions 430 and 431 becomes higher than that of phosphorus in those regions by  $3 \times 10^{17}$  to  $4 \times 10^{18}$  atoms/cm<sup>3</sup>.

As shown in FIG. 4G, after the resist mask 214 is removed, laser annealing is performed to activate the introduced impurities and to restore the crystallinity of the island-like silicon regions 405 and 406 that have been damaged in the doping steps.

In this embodiment, the N-type or P-type source and drain regions 417, 418, 428 and 429 are doped with phosphorus at a concentration of  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>, and the N-type or P-type lightly doped regions 423, 424, 430 and 431 are doped with phosphorus at a concentration of  $4 \times 10^{16}$  to  $7 \times 10^{17}$  atoms/cm<sup>3</sup>. Therefore, nickel can be effectively getter by phosphorus upon laser light illumination.

Where KrF excimer laser light (wavelength: 248 nm) is used, to getter nickel effectively, it is preferred that the laser light illumination conditions be such that the energy density to 200 to 400 mJ/cm<sup>2</sup>, for instance, 250 mJ/cm<sup>2</sup>, each point receives 2 to 20 shots of laser light, and the substrate temperature during the laser light illumination is set at 200° C.

After the laser annealing, thermal annealing is performed at 350° C. for 2 hours in a nitrogen atmosphere. Although both laser annealing and thermal annealing are performed in this embodiment, only one of those may be performed.

As shown in FIG. 4H, a 1-μm-thick silicon oxide film as an interlayer insulating film 432 is deposited by plasma CVD, and contact holes are formed therein. Source and drain electrodes/wiring lines 433 to 435 are formed through the contact holes by using a metal material such as a multi-layer film of a titanium film and an aluminum film. Finally, a heat treatment is performed at 350° C. for 2 hours in a hydrogen atmosphere. With the above steps, CMOS thin-film transistors are completed. (FIG. 4H)

Although in this embodiment boron ions are introduced after the phosphorus ion implantation, they may be introduced before the phosphorus ion implantation. In the latter case, as shown in FIG. 4F, boron ions are introduced in a state that the N-type TFT region is covered with a resist mask 427. Phosphorus ions may be introduced after the resist mask 427 is removed.

The invention enables formation of thin-film transistors in which off-currents are small and variations in characteristics are small, even with the use of a crystalline silicon film into which a catalyst element for accelerating crystallization has been introduced.

In particular, where nickel is used as the catalyst element for accelerating crystallization, the above effects of the invention is remarkable. The above effects are particularly advantageous in forming a plurality of devices having the same functions on the same substrate. This is because an

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off-current variation among devices causes unevenness in characteristics among the devices. Such unevenness is particularly harmful to pixels that are formed in a TFT liquid crystal display device. Thus, the invention is believed very useful in the industrial point of view.

What is claimed is:

1. A method for fabricating a CMOS transistor having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising:

forming a semiconductor film on a insulating surface;  
providing said semiconductor film with a catalyst for promoting crystallization thereof;  
crystallizing said semiconductor film;  
etching said crystallized semiconductor film to form at least first and second semiconductor islands on an insulating surface;

forming a gate insulating film covering each of said first and second semiconductor islands;

forming first and second gate electrodes over each of said first and second semiconductor islands respectively with said gate insulating film interposed therebetween;

first anodizing each of said first and second gate electrodes to form a first anodic oxide film on side surfaces of each said of said first and second gate electrodes;

selectively removing exposed portions of said gate insulating film using each of said first and second gate electrodes and said first anodic oxide film as a mask;

removing said first anodic oxide films after said selectively removing said exposed portions of said gate insulating film, in order to expose other portions of said gate insulating film on each of said first and second semiconductor islands;

forming a first pair of regions in said first semiconductor island by introducing an n-type impurity to form first source and drain regions in said first semiconductor island wherein said n-type impurity is phosphorous;

forming a second pair of regions in said first semiconductor island by introducing said n-type impurity to form lightly doped drain regions in said first semiconductor island, said second pair of the regions in said first semiconductor island being located adjacent to said first pair of the regions in said first semiconductor island;

forming a third pair of regions in said second semiconductor island by introducing said n-type impurity;

forming a fourth pair of regions in said second semiconductor island by introducing said n-type impurity, said fourth pair of the regions being located adjacent to said third pair of the regions;

masking only said first semiconductor island with a resist;

inverting a conductivity type of said third pair of regions by introducing a p-type impurity to form second source and drain regions of said second semiconductor island;

inverting a conductivity type of said fourth pair of regions by introducing said p-type impurity to form second lightly doped drain regions, to thereby form a CMOS transistor having said n-channel thin film transistor in said first semiconductor island and said p-channel thin film transistor in said second semiconductor island; and

activating said n-type impurity and said p-type impurity in said first and second semiconductor islands so that the catalyst is gettered by said n-type impurity.

2. A method according to claim 1 further comprising second anodizing each of said first and second gate elec-

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trodes to form a second anodic oxide film on each of first and second said gate electrodes.

3. A method according to claim 1 wherein said p-type impurity is boron.

4. A method according to claim 1 wherein said semiconductor film comprises silicon.

5. A method according to claim 4 wherein said semiconductor film is amorphous.

6. A method of manufacturing a complementary semiconductor device having at least an n-channel thin film transistor and a p-channel thin film transistor, comprising:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

providing said semiconductor film with a metal containing material, wherein said metal is capable of promoting crystallization of amorphous silicon;

heating said semiconductor film and said metal containing material in order to crystallize said semiconductor film;

patterning the crystallized semiconductor film into at least first and second semiconductor islands, each including a channel formation region;

forming a gate electrode over said first and second semiconductor islands with a gate insulating film interposed therebetween;

introducing phosphorus into both of said first and second semiconductor islands by at least in part using said gate electrodes as masks, thereby at each of said first and second semiconductor islands forming a pair of lightly doped regions that are adjacent to said channel region and opposing each other with respect to said channel region and a pair of heavily doped regions each located on one side of said channel region and in direct contact with one of said lightly doped regions, wherein said heavily doped regions are doped at a first concentration and said lightly doped regions are doped at a second concentration smaller than said first concentration by a first difference amount; and

introducing boron into only one of said first and second semiconductor islands by using at least in part said gate electrode as a mask to dope said heavily doped regions at a third concentration and said lightly doped regions at a fourth concentration larger than said second concentration, said third concentration being larger than said fourth concentration by a second difference amount that is smaller than said first difference amount; and

activating the phosphorus introduced in said first and second semiconductor islands in order to getter the metal residing therein.

7. The method according to claim 6 wherein the activation is conducted by heating.

8. The method according to claim 6 wherein said first concentration is  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup> and said second concentration is  $4 \times 10^{16}$  to  $7 \times 10^{17}$  atoms/cm<sup>3</sup>.

9. A method according to claim 6 wherein said metal is selected from the group consisting of nickel, platinum, cobalt, iron, and palladium.

10. A method of manufacturing a complementary semiconductor device having at least an n-channel thin film transistor and a p-channel thin film transistor, comprising:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

providing said semiconductor film with a metal containing material for promoting crystallization of said semiconductor film;

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crystallizing said semiconductor film;

patterning the crystallized semiconductor film into at least first and second semiconductor islands, each including at least a channel formation region;

selectively introducing phosphorus into both of said first and second semiconductor islands to form a pair of lightly doped regions that are adjacent to said channel formation region and opposing each other with respect to said channel formation region and a pair of heavily doped regions each located on one side of said channel formation region and in direct contact with one of said lightly doped regions, wherein said heavily doped regions are doped at a first concentration and said lightly doped regions are doped at a second concentration smaller than said first concentration by a first difference amount;

selectively introducing boron into only one of said first and second semiconductor islands to dope said heavily doped regions at a third concentration and said lightly doped regions at a fourth concentration layer than said second concentration, said third concentration being larger than said fourth concentration by a second difference amount that is smaller than said first difference amount; and

activating said phosphorus and boron introduced in said first and second semiconductor islands.

11. The method according to claim 10 wherein the activation is conducted by heating.

12. The method according to claim 10 wherein said first concentration is  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup> and said second concentration is  $4 \times 10^{16}$  to  $7 \times 10^7$  atoms/cm<sup>3</sup>.

13. A method according to claim 10 wherein each of said n-channel transistor and said p-channel transistor is of a top-gate type.

14. A method according to claim 10 wherein said metal is selected from the group consisting of nickel, platinum, cobalt, iron, and palladium.

15. A method of manufacturing a p-type semiconductor device comprising:

forming a semiconductor film comprising amorphous silicon on an insulating surface;

providing said semiconductor film with a catalyst material wherein said catalyst material contains a metal for promoting crystallization of silicon;

crystallizing said semiconductor film by heating;

patterning the crystallized semiconductor film into at least first and second semiconductor islands, each having at least a channel formation region;

introducing phosphorus into said first and second semiconductor islands to form n-type impurity regions by ion doping;

introducing boron into said second semiconductor island to form p-type impurity regions by ion doping; and

activating said phosphorus and boron introduced in said first and second semiconductor islands wherein at least a part of the metal residing in said channel region of the first and second semiconductor islands is gettered by said phosphorus.

16. The method according to claim 15 wherein said phosphorus is added at a concentration  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>.

17. A method according to claim 15 wherein said metal is selected from the group consisting of nickel, platinum, cobalt, iron, and palladium.

18. A method of manufacturing a p-type semiconductor device comprising:

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forming a semiconductor film comprising amorphous silicon on an insulating surface;

providing said semiconductor film with a metal containing material for promoting crystallization of silicon.

crystallizing said semiconductor film by heating;

patterning the crystallized semiconductor film into at least first and second embodiment islands, each having at least a channel formation region;

introducing phosphorus by accelerating ions of a dopant impurity into said first and second semiconductor islands to form a pair of heavily doped region with said channel formation region therebetween and at least one lightly doped region between said channel formation region and one of said heavily doped region;

introducing boron into said second semiconductor island to convert a conductivity type of the pair of heavily doped regions and the lightly doped region in said second semiconductor island into a p-type; and

activating and phosphorus and boron-introduced in said first and second semiconductor islands so that at least a part of the metal is gettered by said phosphorus.

19. A method according to claim 18 wherein a concentration of phosphorus in said lightly doped region is within a range from  $4 \times 10^{16}$  to  $7 \times 10^{17}$  atoms/cm<sup>3</sup>.

20. A method according to claim 18 wherein a temperature of said substrate is maintained at a room temperature during the ion doping of said phosphorus and boron.

21. A method according to claim 18 wherein said first and second semiconductor islands constitute a pair of complementary transistors.

22. The method according to claim 18 wherein a concentration of phosphorus in said heavily doped regions is within a range of  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>.

23. A method according to claim 18 wherein said metal is selected from the group consisting of nickel, platinum, cobalt, iron, and palladium.

24. A method of manufacturing a p-type semiconductor device comprising:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film using a crystallization promoting material added thereto wherein said crystallization promoting material contains a metal;

patterning said semiconductor film to form at least one semiconductor island;

selectively introducing phosphorus into said semiconductor island to form a pair of impurity doped regions by ion doping at a first concentration;

selectively introducing boron into said semiconductor island to form a pair of impurity doped regions by ion doping at a second concentration larger than said first concentration.

activating said phosphorus and said boron to getter the metal contained in said semiconductor island.

wherein a temperature of said substrate is maintained during the ion doping of said phosphorus and boron.

25. A method according to claim 24 wherein said first concentration is within a range from  $3 \times 10^{19}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>.

26. A method according to claim 24 wherein said metal is selected from the group consisting of nickel, platinum, cobalt, iron, and palladium.

27. A method of manufacturing a semiconductor device including at least an N-channel type thin film transistor and a P-channel type thin film transistor complementarily connected to each other, said method comprising:

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forming a semiconductor film comprising amorphous silicon on an insulating surface;

crystallizing said semiconductor film, wherein the crystallization is promoted by a metal added to said semiconductor film;

patterning the crystallized semiconductor film into at least first and second semiconductor islands, each having a channel formation region;

introducing phosphorus by ion doping into said first and second semiconductor islands to form a pair of heavily doped regions with said channel formation region therebetween and at least one lightly doped region between said channel formation region and one of said heavily doped regions;

introducing boron into said second semiconductor island to convert a conductivity type of the heavily doped regions and the lightly doped region in said second semiconductor island into a p-type;

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activating said phosphorus and boron introduced in said first and second semiconductor islands to reduce a concentration of the metal in the channel formation regions of the first and second semiconductor islands; and

forming at least first and second gate electrodes over said channel formation regions of the first and second semiconductor islands.

28. A method according to claim 27 wherein a concentration of phosphorus in said lightly doped region is within a range from  $4 \times 10^{16}$  to  $7 \times 10^{17}$  atoms/cm<sup>3</sup>.

29. A method according to claim 27 wherein a temperature of said substrate is maintained at a room temperature during the ion doping of said phosphorus and boron.

30. A method according to claim 27 wherein said metal is selected from the group consisting of nickel, platinum, cobalt, iron, and palladium.

\* \* \* \* \*